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SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF
[Handotai sochi oyobi sono seizo hoho]

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Claims

1. A semiconductor device characterized in that the source and drain regions of an offset structure MOSFET are constituted with a low-impurity concentration offset part and a main region that stretches outside of that, and in that the main region is formed deeper than the offset part and an insulating film is interposed at the boundary on the substrate side.

2. The semiconductor device described in Claim 1 wherein the main region is formed with a semiconductor material with a high-impurity concentration.

3. The semiconductor device described in Claim 1 wherein the region main pat is formed with a metal or metal silicide.

4. A semiconductor device manufacturing method characterized in that, when the source and drain regions of a MOSFET are formed, an offset part with a low-impurity concentration is formed beforehand, a groove deeper than the offset region is next formed in a semiconductor substrate in a place corresponding to the region main pat, and after an insulating film is formed in the inner surface of the groove, a low resistance material is deposited to constitute a main region.

5. The semiconductor device manufacturing method described in Claim 4 wherein the offset part is formed with self matching using a gate electrode, a side wall is next formed on the gate electrode, and the groove for the main region is formed by etching using that [side wall] as a mask.

6. The semiconductor device manufacturing method described in Claim 4 or 5 characterized in that the groove inner surface is oxidized for an oxide film, and the oxide film is formed as an insulating film.

Detailed explanation of the invention

Technical field

The present invention relates to a semiconductor device and manufacturing method thereof that enables high-sped operation, and at the same time, enables higher integration and improved breakdown voltage.

Background art

Semiconductor devices, e.g., IC and LSI, in recent years have achieved increasing higher integration, and with MOSFETs (MOS type field-effect transistor) shorter channels have been achieved. However, when channels are shortened, the source and drain regions must be made shallower to prevent side effects, such as threshold gate length dependence, that occur because of so-called short channel effects. The resistance of the source and drain regions becomes larger, which hinders higher speed by the element. Also along with shorter channel length, problems also occur with breakdown voltage, and in the past, a lightly doped drain structure with a profile wherein the source and drain regions comprise a high-concentration main region and a low-concentration region, has been proposed (IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. ED-29, NO. 4, APRIL 1982, P 590-FF). However, the main region wherein resistance is relatively small has become even tinier, and augments the higher resistance described above. And because parts of particularly high concentration in the source and drain regions are constituted directly contacting a well or substrate of the opposite conductive type, junction capacitance becomes larger, and when it is used for a C-MOS structure, there are obstacles to higher integration, e.g., latch-up and breakdown voltage become lower, and element separation dimensions must be made larger.

Objective of the invention

The objective of the present invention is to provide a semiconductor device that achieves lower resistance by the source and drain regions of a MOSFET that achieves shorter channels to enable higher speed, that also enables improved breakdown resistance and reduced junction capacitance, and that can achieve higher integration, in addition.

Another objective of the present invention is to provide a manufacturing method suited to the semiconductor device described above that is capable of high-speed operation and that achieves higher integration.

The abovementioned and other objectives of the present invention and new features will become clear from the description in this specification and from the attached figures.

Summary of the invention

The summary of a representative one of the inventions disclosed in this application is presented below and explained briefly.

In short, by using a constitution wherein the main region in the source and drains regions of a MOSFET formed in an offset structure are formed deep, and an insulating film is interposed at the boundary of the main region and the substrate side, improved breakdown voltage makes the apparent depth of the source and drain regions larger; lower resistance, that is, higher speed, is achieved, decreased junction capacitance is additionally achieved, and higher integration is furthermore achieved using shorter channels.

And by forming a groove in the place for the main region after the offset place for the source and drain regions is formed, forming an insulating film on the surface of the groove, and then depositing a

conductive material in the groove, a structure for a semiconductor device of the abovementioned high-speed operating type and highly integrated type is accomplished.

Application example

Figure 1 shows an application example wherein a semiconductor device in the present invention is applied to n type MOSFET (1). In short, a field insulating film (3) formed using selective oxidation (LOCOS) is furnished on the principal surface of a p type silicon semiconductor substrate (2) to define the active region, and N-MOSFET (1) is constituted in the active region. N-MOSFET (1) comprises a gate electrode (5) formed on gate insulating film (4), and source and drain regions (6) and (6) doped with an n type impurity. The source and drain regions in particular are formed with low impurity concentration (n^-) portions (7) and (7), and high impurity concentration (n^+) main regions (8) and (8) continuing to the outside of them. Aforementioned main regions (8) and (8) are formed deeper toward the inside of substrate (2) to achieve lower resistance. Insulating films (9) and (9) composed of silicon oxide films (SiO_2 films) are also formed at the boundaries of main regions (8) and (8) and substrate (2), and reduced junction capacitance is achieved in main regions (8) and (8). In the figure (10) and (11) are SiO_2, and PSG interlayer insulating films (12) and (12) are Al wiring.

Next, the manufacturing method for N-MOSFET (1) with the constitution above is explained based on the process diagrams in Figures 2 (A)-(I).

First, a field insulating film (SiO_2) (3) is formed using LOCOS on the principal surface of a p type silicon substrate (2) to define the active region, a gate insulating film (SiO2) (4) is formed on the active region, and then after a polysilicon layer is formed on that, a gate electrode (5) is formed by it [polysilicon layer] as shown in Figure 2 (A). After this, the substrate principal surface is doped with phosphorus (P) as

the impurity using self matching, and low concentration n^- layers (7a) and (7a) corresponding to offset parts (7) and (7) are formed.

Next, as in the same figure (B), a silicon nitride film (Si_3N_4) (13) and an SiO_2 film (14) are formed over the entire surface using CVD. By next etching them off using reactive ion etching (RIE), sidewalls (15) and (15) are formed on both sides of gate electrode (5) as in the same figure (C). In this case, if SiO_2 film (14) is formed relatively thick, a certain amount of SiO_2 film (14) and Si3N4 film (13) can be left on gate electrode (5), depending on the relationship of the sectional shape of gate electrode (5) and the RIE. Then grooves (16) and (16) of the same depth as aforementioned n^- layers (7a) and (7a) are formed by etching in source and drain regions (6) and (6) using sidewalls (15) and (15) as masks.

Next, an Si_3N_4 film (second Si_3N_4 film) (17) and an SiO_2 film (second SiO_2 film) (18) are again formed over the entire surface using CVD, and by etching them using RIE, second sidewalls (19) and (19) are formed on both sides of aforementioned sidewalls (15) and (15) and the inner vertical surfaces of aforementioned grooves (16) and (16) as in the same figure (D). Then, substrate (2) is again etched using second sidewalls (19) and (19) as masks, and even deeper new grooves (20) and (20) are formed as in the same figure (E) in the undersides of aforementioned grooves (16) and (16).

Next, as in the same figure (F), after second SiO_2 film (18) is etched off, the inner surfaces of grooves (20) and (20) are oxidized to form oxide films (9) and (9) as insulating films. In this case, the side surfaces of regions (7) and (7) are covered with second Si_3N_4 films (17) and (17), so no oxide film is formed. In addition, after second Si_3N_4 films (17) and (17) are removed, polysilicon (8a) doped with an n type impurity to a high concentration is deposited over the entire surface as in the same figure (G). In this case, grooves (20) and (20) are filled with polysilicon (8a). Then, if polysilicon (8a) is etched from the surface, only polysilicon (8a) in aforementioned grooves (20) and (20) is left, and main regions (8) and (8) with a high concentration of impurity (n^+) are constructed. Main regions (8) and (8) are connected with

aforementioned offset part (7) and (7) with a low concentration of impurity, and source and drain regions (6) and (6) are formed by main region parts (8) and (8) and regions (7) and (7) because of this.

In addition, Si_3N_4 film (13) and SiO_2 film (14) on gate electrode (5) are removed, oxidation treatment is again applied, and an SiO_2 film (10) is formed on gate electrode (5) and source and drain region (6) and (6) as in the same figure (I). If a PSG film (11) is additionally formed on this, and Al wiring (12) and (12) are formed after contact hole formation, N-MOSFET (1) in Figure 1 can be completed.

With N-MOSFET (1) formed as above, source and drain regions (6) and (6) are formed with low impurity concentration regions (7) and (7) and high concentration main regions (8) and (8), and are constituted with gate electrode (5). Therefore, even when the channels are shortened, the breakdown voltage can be made high. At the same time, because of the structure of source and drain regions (6) and (6), the depth of main regions (8) and (8), which occupy a large portion of the region, can be made lager, so lower resistance can be achieved and higher speed can be realized. In this case, regions (7) and (7) are as conventionally, and the side effect of gate length dependence of the threshold value that accompanies shorter channels does not occur. In addition, because insulating films (9) and (9) are formed at the boundaries of main regions (8) and (8) and substrate (2), the overall junction capacitance of source and drain regions (6) and (6) can be reduced. Ultimately, the various problems that accompany shorter channels can be prevented, element miniaturization can be achieved, and higher integration can be achieved.

Here, insulating films (9) and (9) of main regions (8) and (8) can also be used as insulating films to separate elements, and therefore, 2 MOSFETs (1A) and (1b) as in Figure 3 can be disposed adjacent. When this structure is applied to a C-MOS device comprising an N-MOSFET (1A) and a P-MOSFET (1B) formed on p well (21) and n well (22) as in the same figure, in addition to higher integration and

higher speed, improved latch-up and breakdown voltage are also enabled. In Figure 3, the same symbols are assigned to the portions corresponding to Figure 1.

Effect

(1) The source and drain regions of the MOSFET have an offset structure comprising a low impurity concentration region and a main region, so improved breakdown voltage can be achieved.

(2) Only the main region of the source and drain regions can be formed deep, so the side effect of gate length dependence of the threshold value accompanying shorter channels can be prevented. At the same time, lower resistance of the source and drain regions can be achieved, and higher speed can be achieved.

(3) Because an insulating film is formed at the boundary of the main region and the substrate, reduced junction capacitance can be achieved, higher speed is enabled, and more stable operation can also be achieved.

(4) Because improved breakdown voltage, higher speed, etc. can be achieved with using shorter channels, element miniaturization is promoted and higher integration can be achieved.

(5) Grooves are formed with etching technology using gate electrode self matching, insulating films are formed using oxidation technology in the groove inner surfaces, and the source and drain main regions can be formed using polysilicon deposition and etching technology. So no special technology is required, and it is possible to manufacture semiconductor devices with high breakdown voltage, high speed and high integration without significantly increasing the number of processes compared to conventional MOSFET manufacturing processes.

The invention devised by the present inventor was explained above in concrete terms based on an application example, but it goes without saying that the present invention is not limited to the aforementioned application example and various modifications are possible within a scope not deviating

from its essential points. For example, in place of high impurity concentration polysilicon, the main region of the source and drain regions could also use a metal silicide, and lower resistance can be improved even further. Selective etching using photolithography could also be used for groove formation. In addition, various methods other than CVD can be used for the formation methods for the various films and for the polysilicon deposition method.

Fields of application

In the explanation above, a case wherein the inventive device of the present inventor was applied to a basic MOSFET, which is the background field of application, was explained, but this is not limiting. [The invention] can be applied to all ICs or LSIs using a MOSFET as an element, and can be applied particularly effectively to high-speed, highly integrated type semiconductor devices.

Brief description of the figures

Figure 1 is a cross section of an application example of the present invention,

Figures 2 (A)-(I) are cross sections of manufacturing processes,

Figure 3 is a cross section of a variant example.

(1), (1A), (1B) ... MOSFET, (2) ... semiconductor substrate, (3) ... field insulating film, (4) ... gate insulating film, (5) ... gate electrode, (6) ... source and drain region, (7) ... low impurity concentration region, (8) ... main region, (9) ... insulating film, (10) ... SiO_2 film, (11) ... PSG film, (15) ... sidewall, (16) ... groove, (19) ... second sidewall, (20) ... groove, (21) ... p well, (22) ... n well.

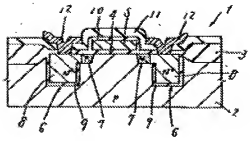

Figure 1

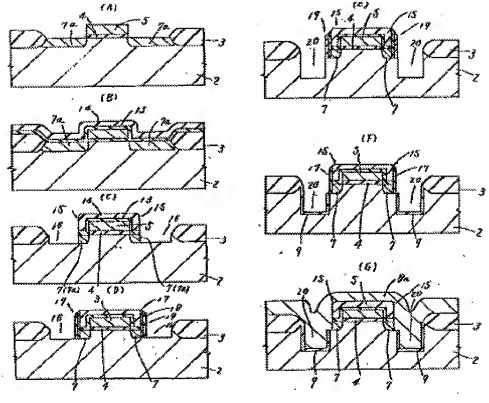

Figure 2

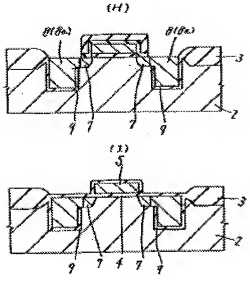

Figure 2 (cont.)

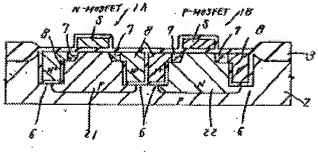

Figure 3